

FIGURE 1

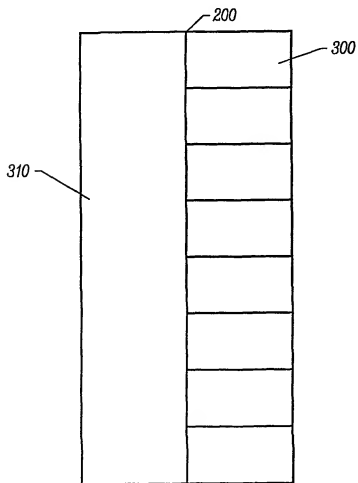


FIGURE 4

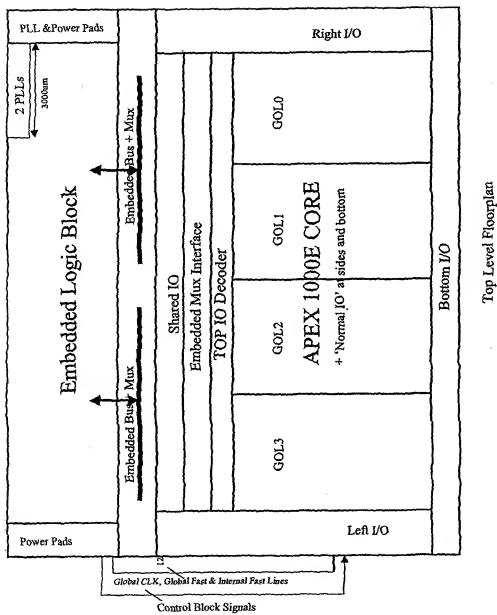


FIGURE 2

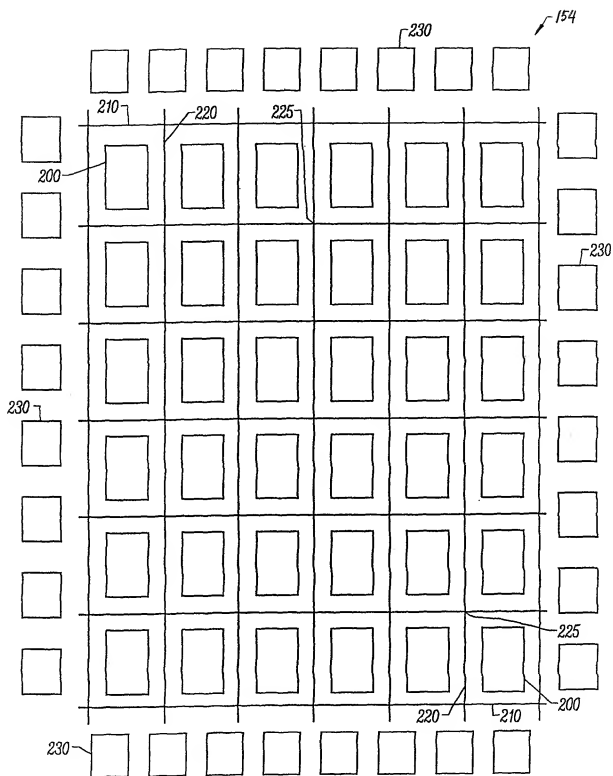


FIGURE 3

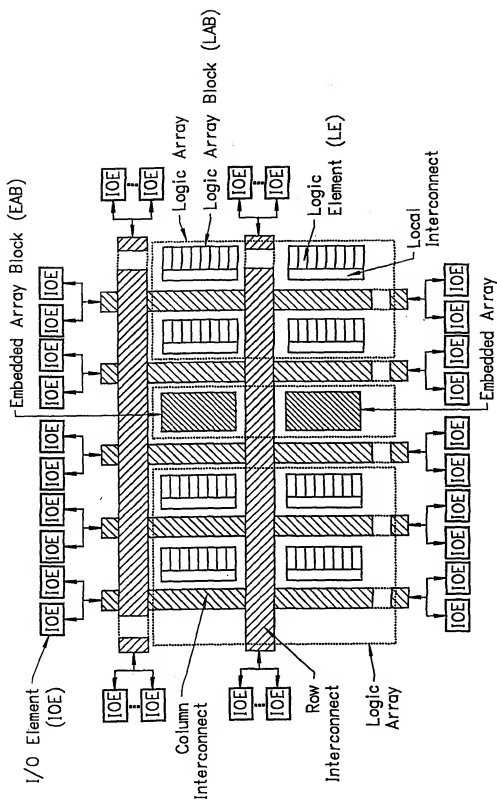


FIGURE 5

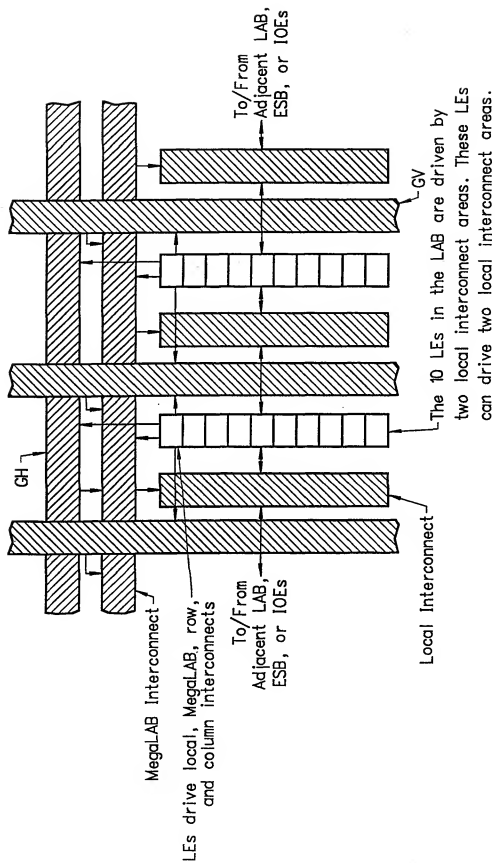


FIGURE 6

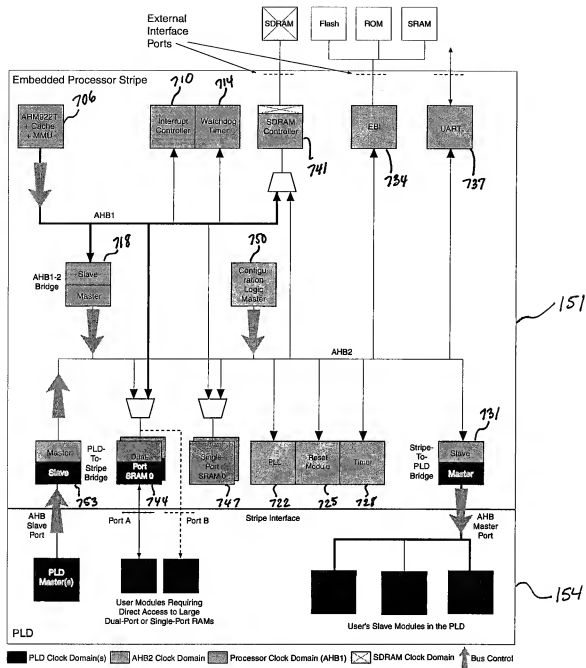


FIGURE 7

FIGURE 8

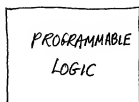


FIGURE 9

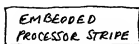


FIGURE 10

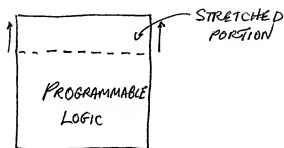
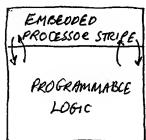


FIGURE 11



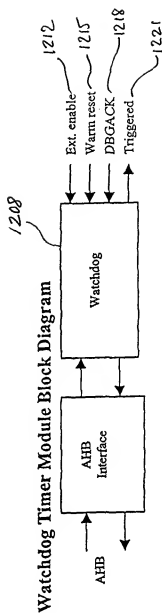


FIGURE 12

Control Register (WDOG_CR) – Read/Write

Register : WDOG_CR Address : Address Base + 0x4C0

Access: Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		TRIGGER																													
LK		0																													

LK When this bit has the value 1 further writes to the register have no effect.

TRIGGER R/W 0 means watchdog disabled. Other values specify bits 29:4 of the trigger value (bits 3:0 of the trigger are always zero.

0 R Reserved for future use. Write as 0 to ensure future compatibility.

FIGURE 13

Count Register (WDOG_COUNT) – Read Only

Register : WDOG_COUNT Address : Address Base + 0x4C4 Access: Read

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

COUNT R Current value of watchdog count register.

FIGURE 14

Reload Register (WDOG_RELOAD) – Write Only

Register : WDOG_RELOAD Address : Address Base + 0x4C8 Access: Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAGIC																															

MAGIC W Magic value to reset watchdog.

FIGURE 15

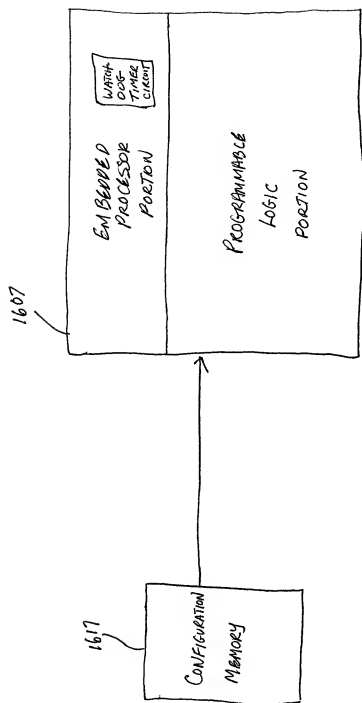


FIGURE 16

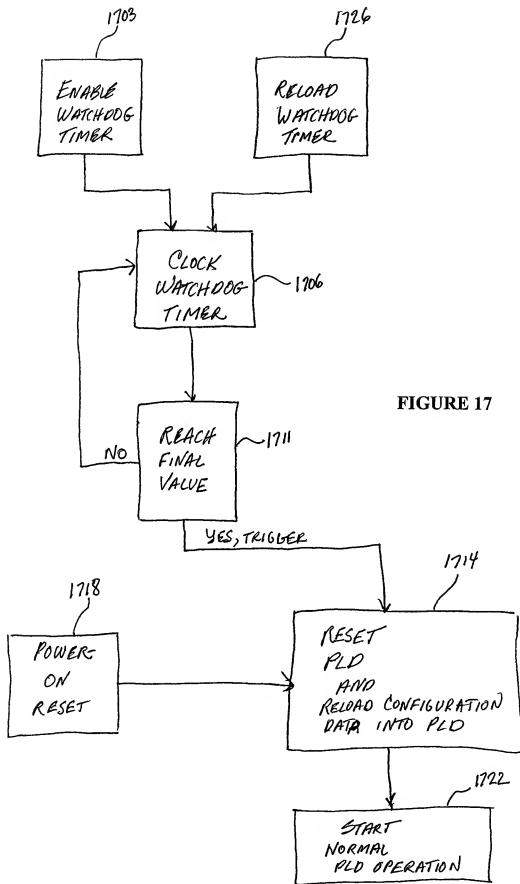


FIGURE 17